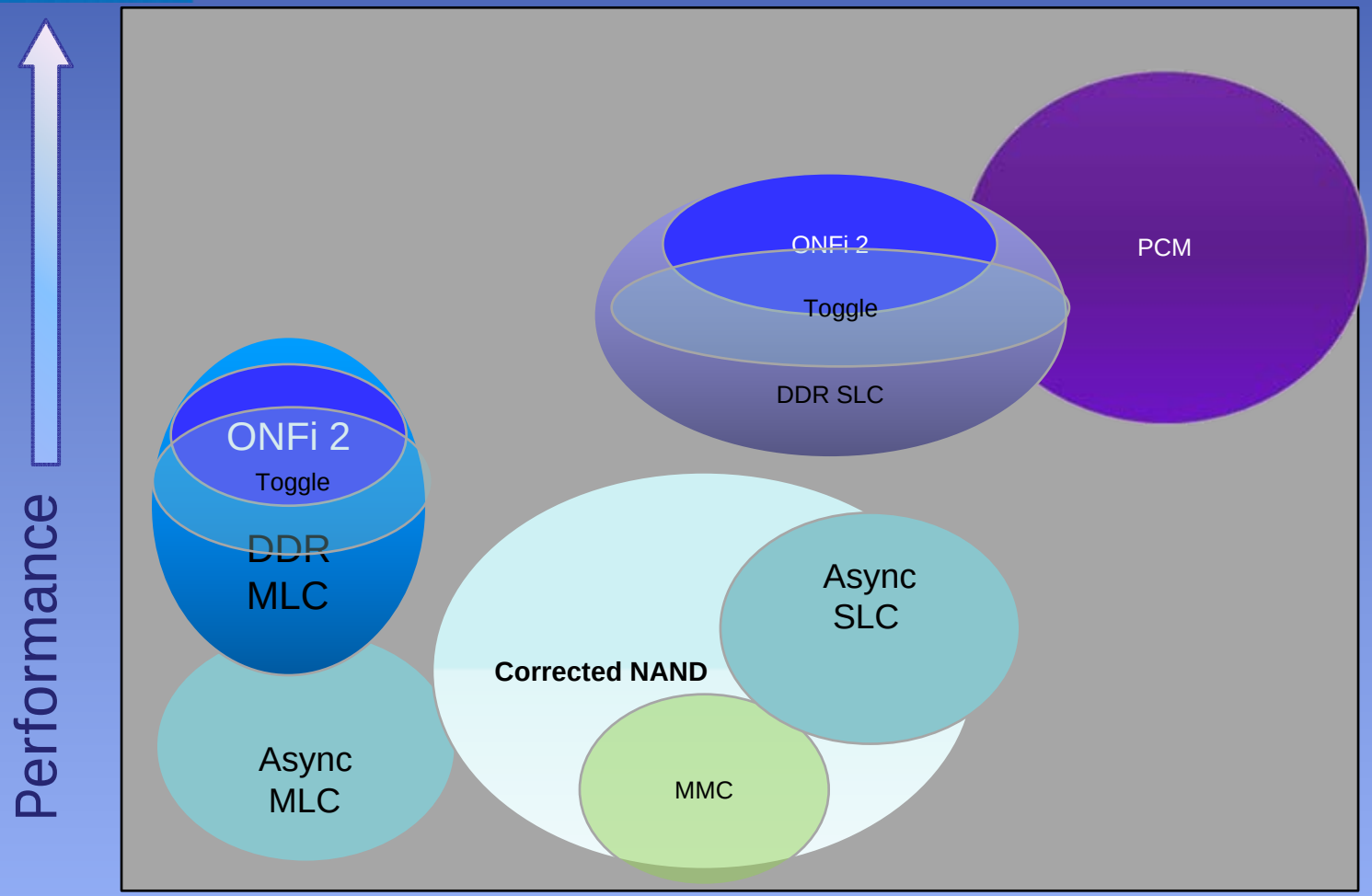
Five Key Steps to High-Speed NAND Flash Performance and Reliability

Presenter

Bob Pierce

NVM Performance Trend



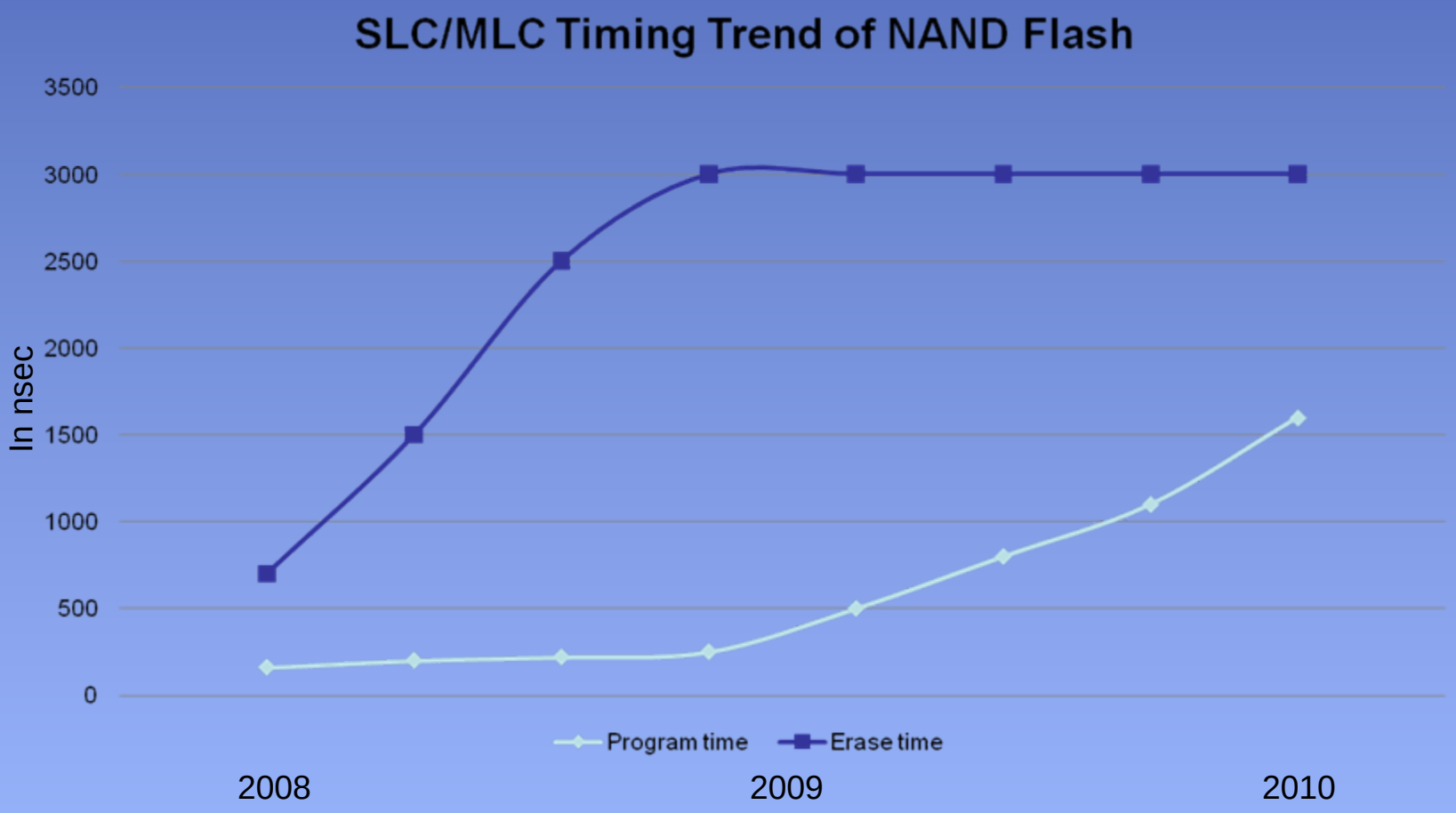
Five Steps to obtaining NAND Reliability and Performance

1. Utilizing Device commands and parameters
2. Architecture advancements
3. Error correction improvements
4. Maximizing Interface performance
5. Using Software and hardware to maximize objectives

Keys to Flash Device Performance

- Page Size increases
  - 2,4,8 K page size What is the impact to bit growth and addressing?
- Read, Write Cycles have been pretty stable
  - From 30 to 6 nsec range
- Key Timing Parameters
  - Trc, Twc, Tprog, Tr, Tbers

Critical Timing of NAND Flash



Command and Architecture Improvements

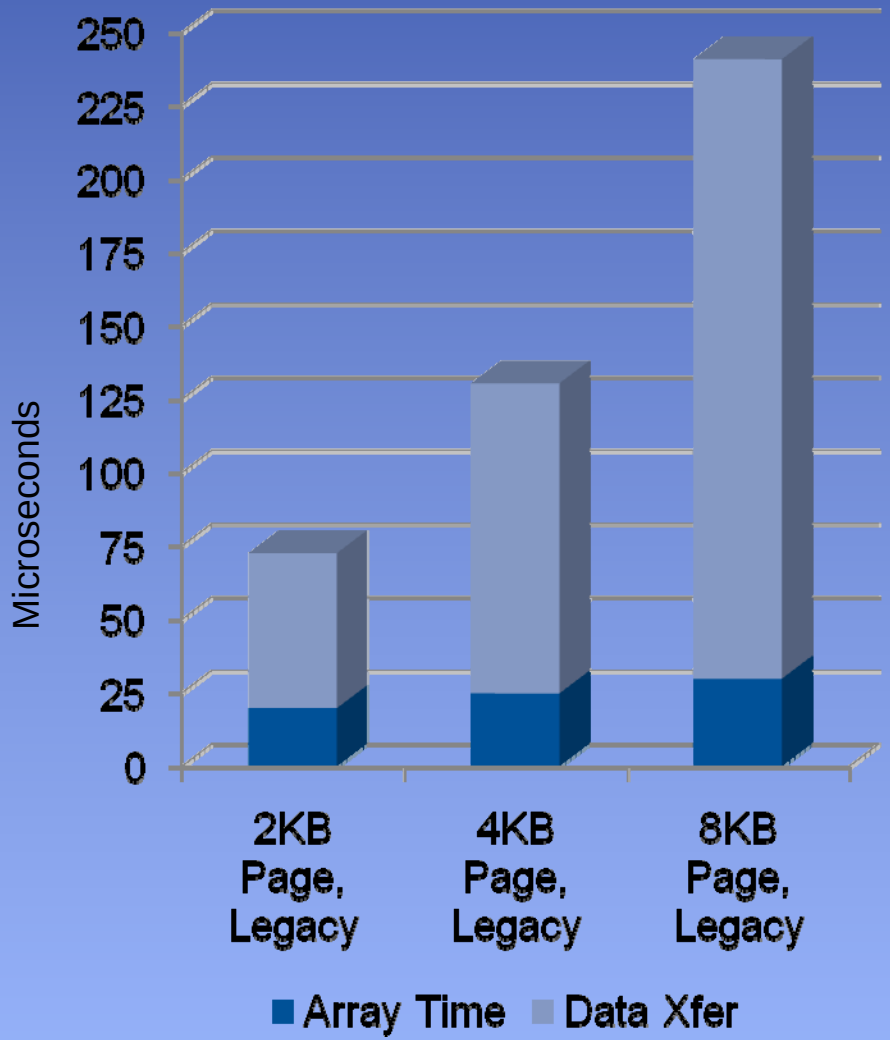
- Multi Plane
- Bus turn-around time
  - Ability to transfer data
  - Multi device switch performance
- LUN Addressing
- Multiple Access capability
  - LUN addressing
  - Volume Support

- Cache Read
- Cache write
- Pipeline read
- Pipeline write
- Enhanced commands
- Higher Bus Speed (Toggle, ONFi 2)

System Performance Benefits

- Enhanced commands
  - Small Data Move command if supported, allows the host to transfer data to the page register in increments that are less than the page size of the device for both Program and Copy back operations.
- Bandwidth
  - Ability to utilize the larger page sizes
- Reducing read and write page access cycles
- Command pipe lining
- Improving read modified write operation

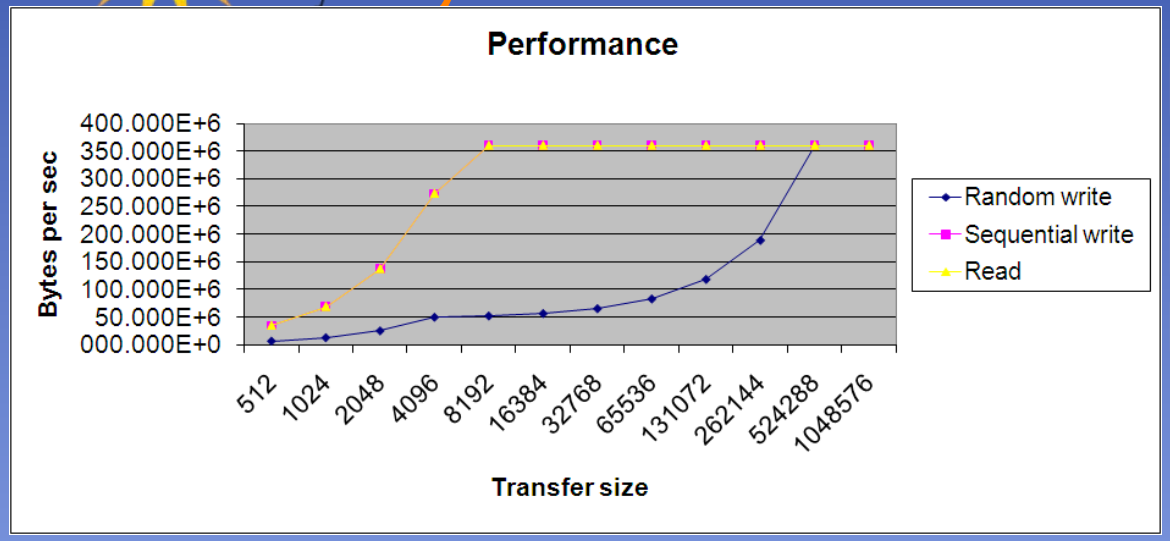
Challenges: Latency Increases as Lithography Shrinks



Data supplied by Micron

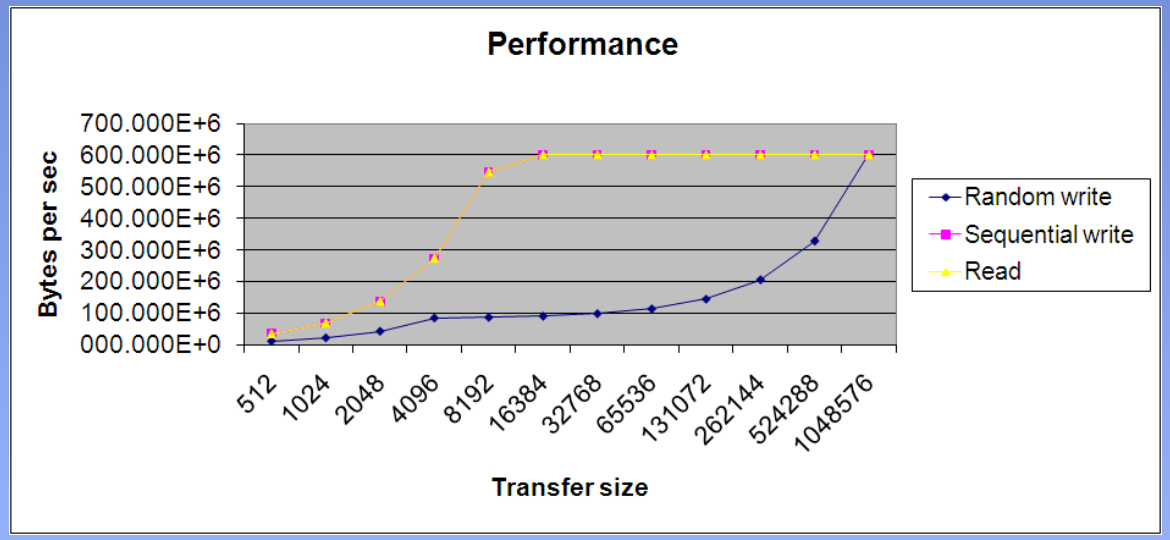
- NAND component performance is determined by two elements:
  - NAND array access time
  - Data transfer across the bus
- I/O time for NAND Page (tRC=20ns)
  - 2K page: 42µs
  - 4K page: 86µs
- For legacy reads, performance is artificially limited to 40 MB/s
  - Today for SLC NAND the I/O time is 2-4x the array transfer time
- As NAND page sizes increase, latency becomes large
  - Especially for small reads
- NAND array read transfer time
  - SLC: tR time is normally 20-25µs MAX
  - MLC: tR time is normally 50µs MAX
- I/O performance must be less than or equal to array performance for maximum sustained read throughput

System Performance



SLC *Asynchronous* Devices

- 8 Chip enables per channel
- 10 Channels or Flash controllers
- 4K Page size
  - Sequential Read 360MBps
  - Sequential Write 360MBps
  - Random Write 52MBps @8K transfer



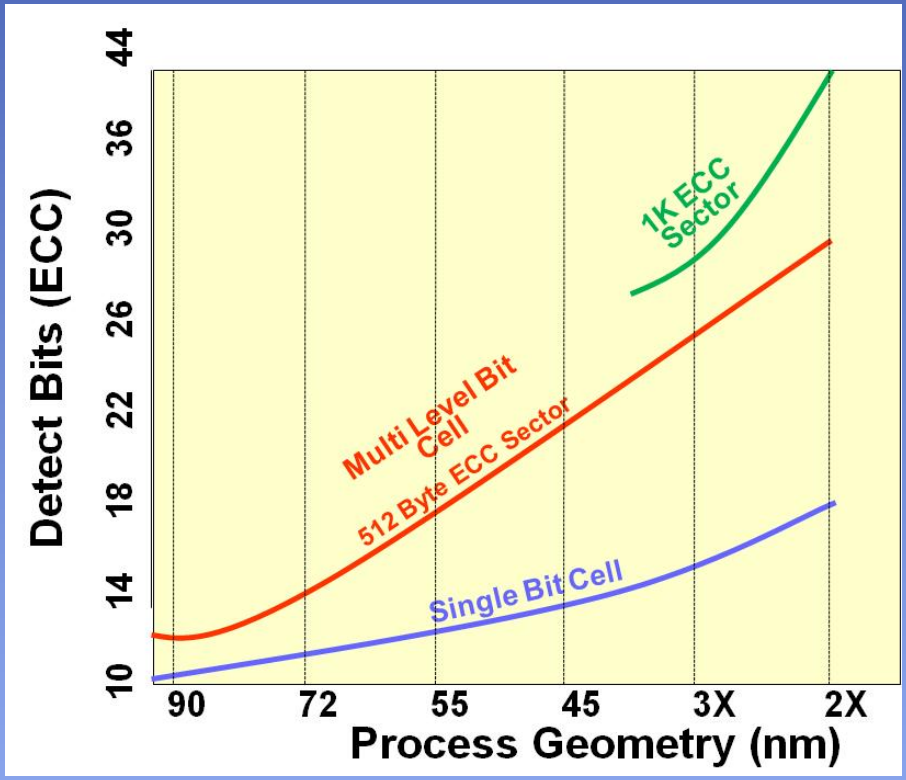
SLC *Synchronous* Devices

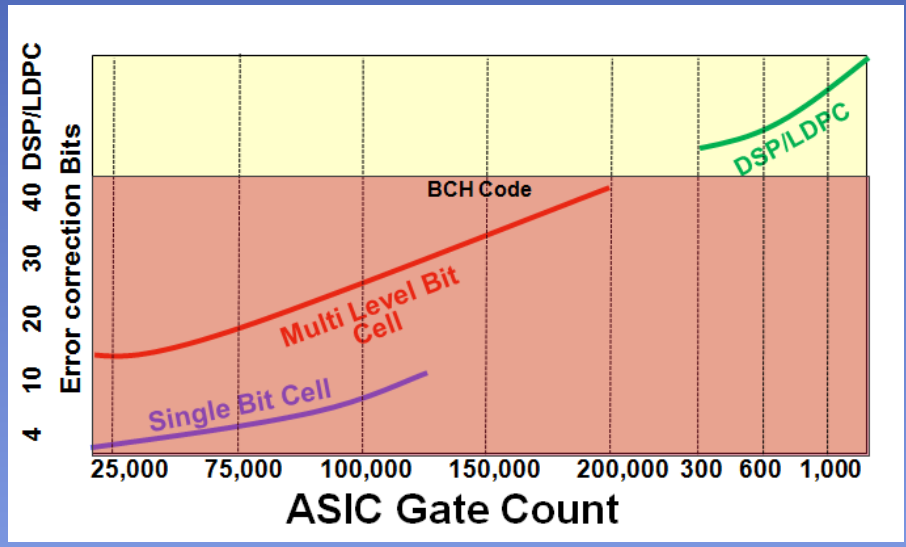
- 8 Chip enables per channel
- 5 Channels or Flash controllers
- 4K Page size
  - Sequential Read 600MBps
  - Sequential Write 600MBps
  - Random Write 86MBps @8K Transfer

Sequential vs. Random Operations

- **Sequential operation typical applications**
  - Card Based solutions USB, MMC etc
  - Storage of data, pictures, videos, boot image
- **Random Operations**
  - Embedded Systems
  - SSD’s
  - Caching
  - Storage of data, active memory access and storage.

ECC Trend



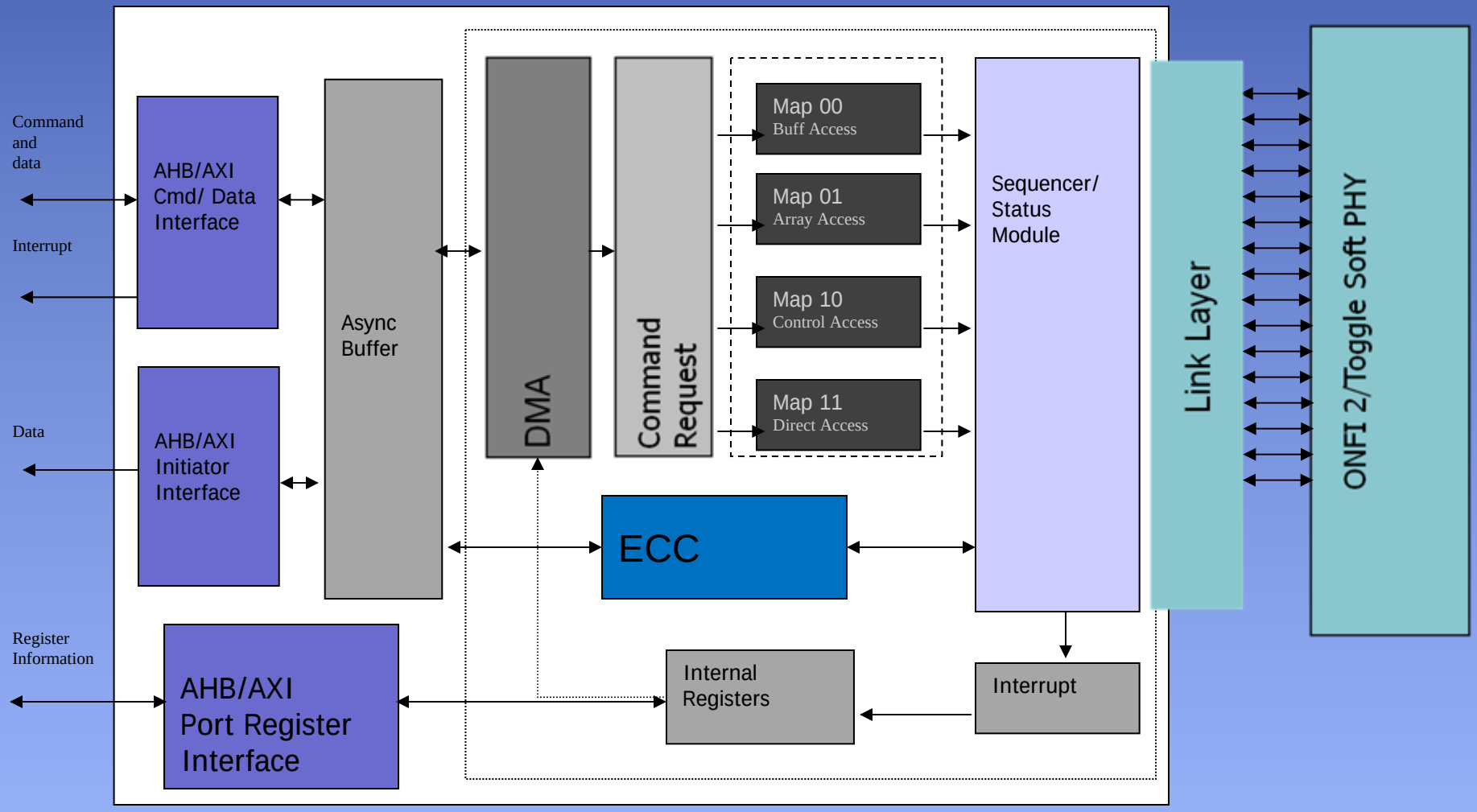


- Typical Controller use more than one type of Error Correction i.e. 8 and 30bits
- DSP and LDPC (Low Density Parity Check Code) are typically high latency Solutions
- BCH (Bose and Ray-Chaudhuri) should be close if not at Line rate.

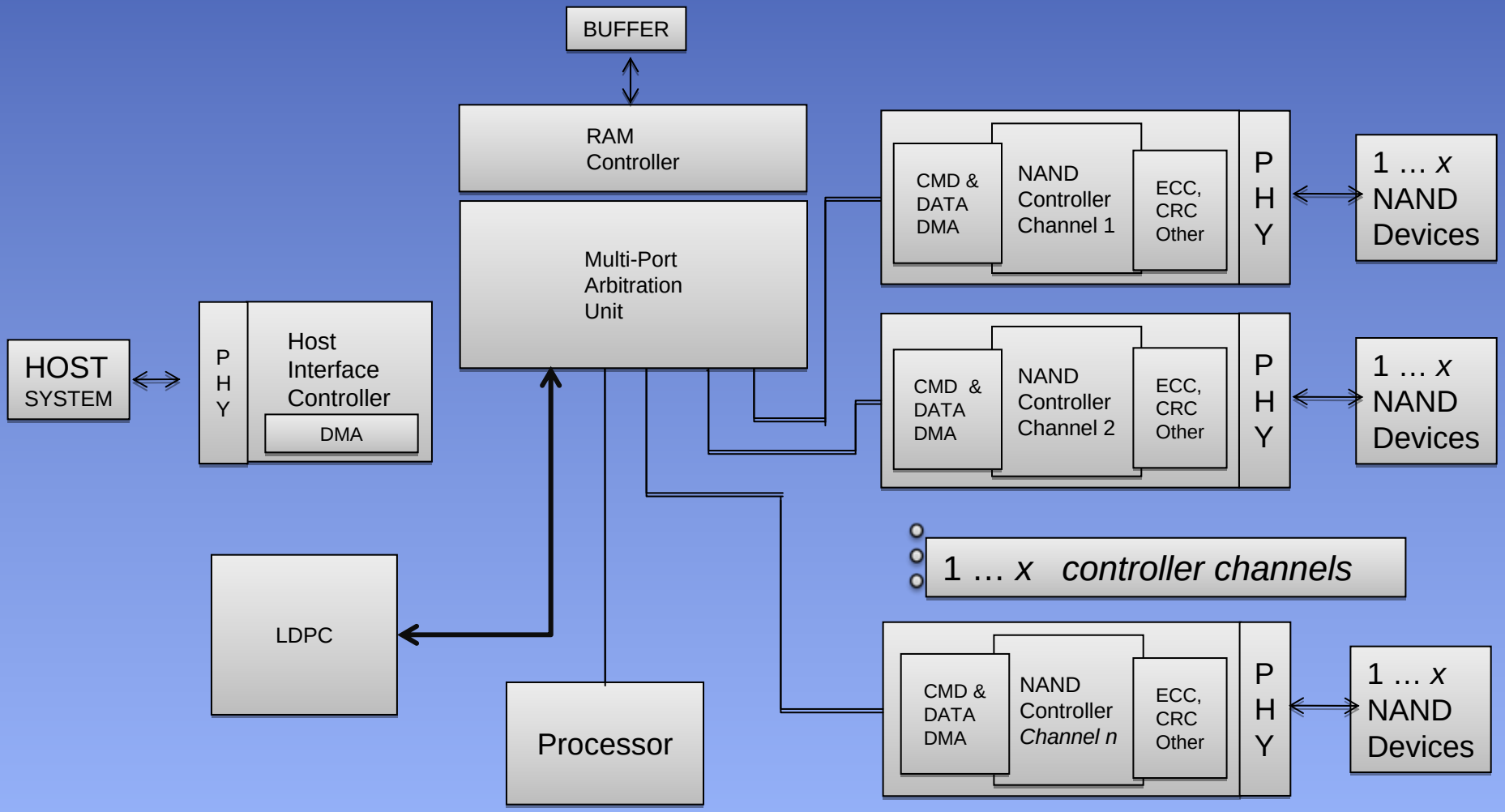
Error Correction Code Comparison

	BCH	Long BCH	LDPC
Latency	Low	Medium	High
Decoder Throughput	Very High	High	Medium
Gate Counts	Small	Medium	Large
Overhead Size	Very Small	Small	Small
Error Correction Capability	Limited	Better	Best

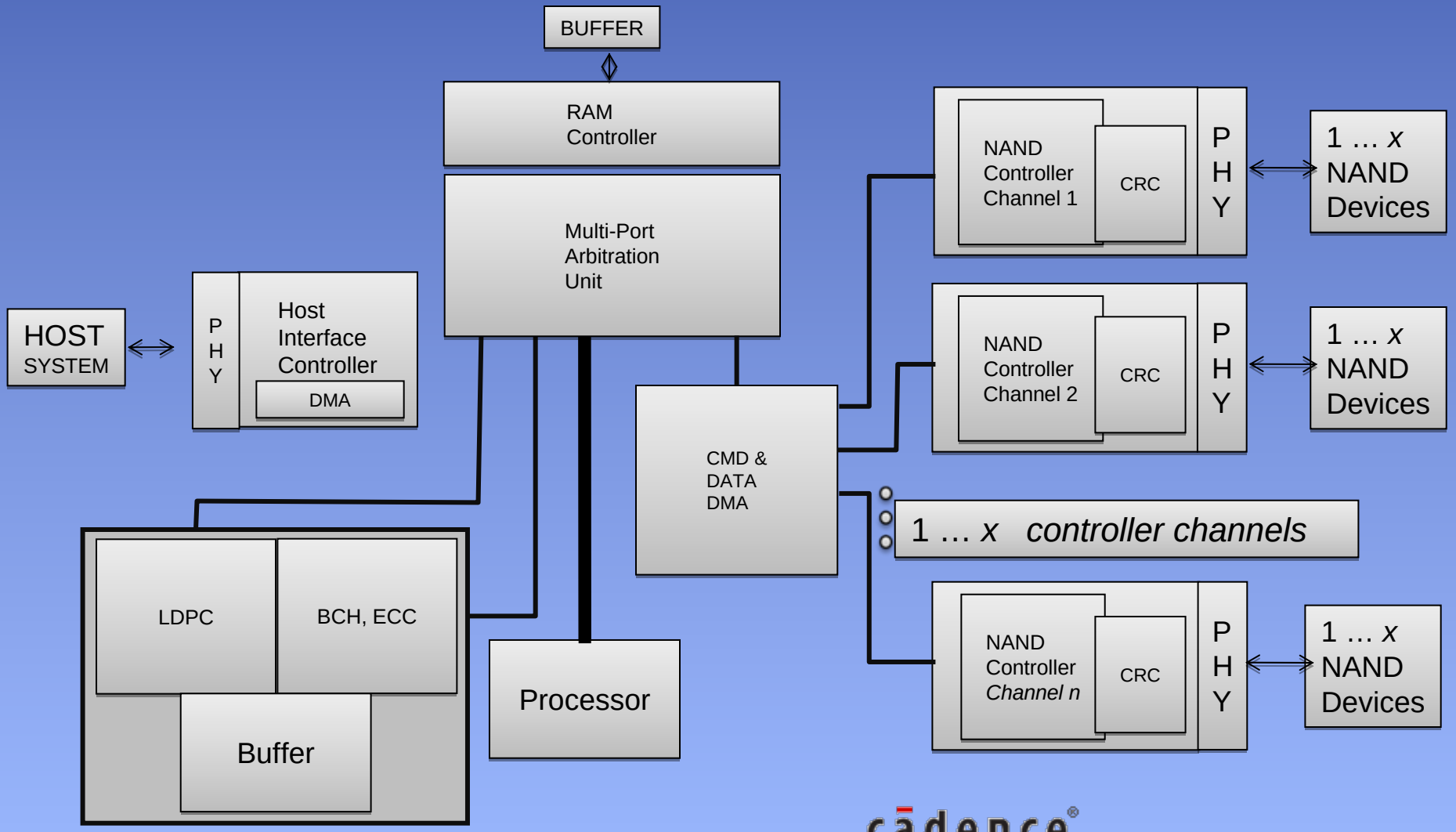
Cadence Nand Controller w PHY Support



Centralized LDPC Hardware Architecture



Centralized ECC Hardware Architecture



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Key Aspects to System Performance Improvements

- Increase the number of commands to the flash device
  - Maximizes the number of transactions that a device can do
  - Toggle NAND is capable of 125% more Read bandwidth over typical asynchronous devices
- Fast error correction and identification of errors
  - Improves block management throughput
  - Reduces processor overhead
- Reduce Interrupts to processor
  - Improves the number of transactions, address translation
  - Improves ECC performance
  - Improves background process operation
  - Removes software timer requirements

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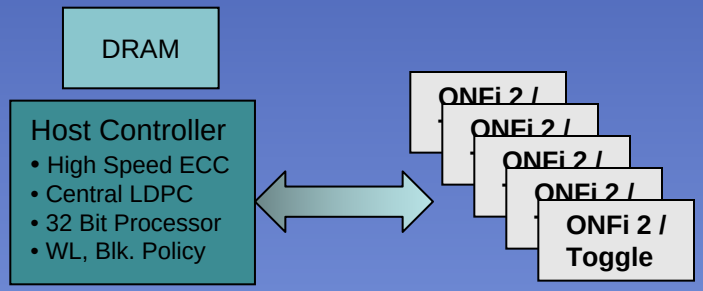
Performance System Architecture

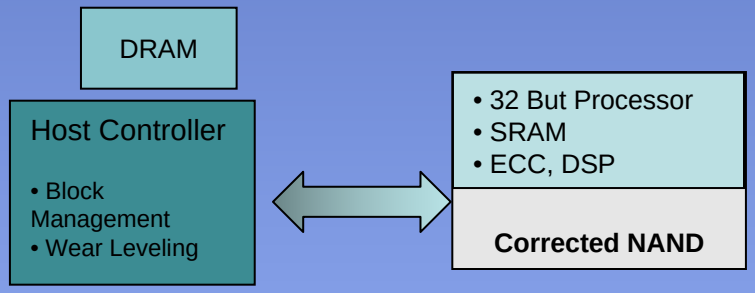
Applications

- **SSD Controller**
- **UFS**
- **Cache Controller**
- **Enterprise**



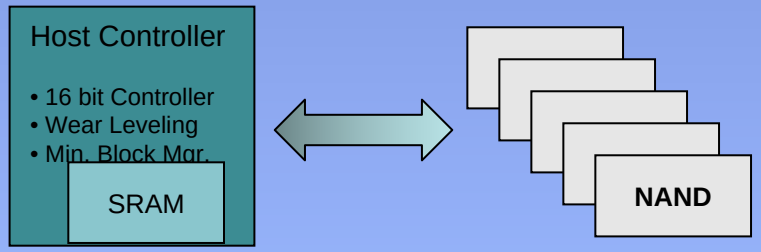
- Highest Performance
- Most flexibility for Block Policy
- Architectural Flexibility
- Highest Error Correction Solution
- Command Q to maximize Bus utilization

- **SSD Controller**
- **HS USB 3.0**
- **Cache Module**



- Reduced HOST Resources
- Known good Data
- Higher data latency
- Easier to keep up with shrink Path
- Less flexible for block policy

- **Card based**
- **USB 2/3**
- **MMC**



- High Latency
- Poor Random performance
- Block management slow
- Hard to keep up with HS Flash
- Basic ECC operation
- Low write count

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Five Trends to watch

1. Nand Device architectures and commands have to continue to improve. Array performance is degrading, command and architecture improvements must continue.
2. ECC Solutions are more complex and have become the corner stone to improved data reliability and Block Policy management.
3. New controller architectures must continue to evolve based on system requirements and complex NAND architectures. (One size not fit all)
4. Interface data rates have to increase to maximize multi chip transfer rates and increase through put. (higher transfer rate)
5. Software complexity utilizing new error correction methods are more complex, NAND management is comprised of multiple solutions all requiring some decision properties.